In the Claims:

Please cancel claims 1-6 and 9-14, and add new claims 15-26:

15. (New) A method of manufacturing a semiconductor integrated circuit comprising the steps of:

employing at least one common mask to form a plurality of functional blocks and a gate array block within predetermined first areas on a surface of a semiconductor chip, said functional blocks being provided respectively with predetermined functions by semiconductor devices and said gate array block including a plurality of unconnected basic cells;

placing a plurality of I/O buffers in a second area surrounding said first area;

designing circuits for inclusion in said gate array block; and

employing at least one circuit mask to establish electrical connections between the basic cells in accordance with the circuits designed in the previous step, whereby the time required to manufacture the semiconductor integrated circuit and the size of said first areas is minimized.

16. (New) The method of manufacturing a semiconductor integrated circuit according to claim 15, wherein the electrical connections established between the basic cells provide at least one logic element.

17. (New) A method of manufacturing a semiconductor integrated circuit according to claim 15, wherein said gate array block is laid out by a standard cell system.

18. (New) A method of manufacturing a semiconductor integrated circuit according to claim 15, wherein said gate array block is laid out by one of a standard cell system and a full custom system.

19. (New) A method of manufacturing a semiconductor integrated circuit according to

claim 15, comprising the further steps of establishing electrical connections between the functional blocks and establishing electrical connections between the functional block and the gate array block.

20. (New) A semiconductor integrated circuit comprising:

a plurality of functional blocks placed on a semiconductor chip, said functional blocks being respectively provided with predetermined functions by semiconductor devices;

a gate array block placed on said chip, said gate array block being comprised of a plurality of electrically connected basic cells, said electrically connected basic cells implementing desired functions, the gate array block having a circuit designed after placing said plurality of functional blocks and said plurality of basic cells on said chip, said functional blocks and said gate array block being laid out with at least one common mask in a first area including a center position on a surface of the semiconductor chip; and

a plurality of I/O buffers surrounding the first area.

21. (New) A semiconductor integrated circuit according to claim 20, wherein a connection between basic cells is in accordance with a standard cell system.

22. (New) A semiconductor integrated circuit according to claim 20, wherein said plurality of functional blocks includes a CPU core block.

23. (New) A semiconductor integrated circuit according to claim 20, wherein said plurality of functional blocks includes a memory cell block.

24. (New) A method of manufacturing a semiconductor integrated circuit comprising the steps of:

a first step of employing at least one common mask to form a plurality of functional blocks and a gate array block within predetermined first areas on a surface of a semiconductor chip, said functional blocks having predetermined functions and said gate array block including a plurality of unconnected basic cells;

a second step of designing a circuit for inclusion in the gate array block; and

a third step of employing at least one circuit mask to establish electrical connections between the basic cells in accordance with the circuit designed in the second step.

25. (New) The method of claim 24, wherein at least part of said second step occurs contemporaneously with said first step.

26. (New) The method of claim 24, wherein the first step is completed prior to beginning the second step.